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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/913,791	08/16/2001	Nobuhiko Kenmochi	110215	4112

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EXAMINER	
GOSHTASBI, JAMSHID	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/913,791	KENMOCHI, NOBUHIKO	
	Examiner	Art Unit	
	Jamshid Goshtasbi-G.	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/16/01,4/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Tomimitsu (US 4777612).

As to **Claim 1**, Tomimitsu discloses a nonrecursive digital filter (Figs 4 and 5; col. 4, lines 17-34) comprising an n-stage (elements 311-31m and 330-33m; col. 4, lines 21-22) shift register that sequentially shifts input data having a predetermined number n of bits (X(nT2); col. 4, lines 35-36), and in which an output of each output stage of the shift register is multiplied (multipliers 321-32m and 341-34m; col. 4, lines 21-26) by a filter coefficient (odd coefficients a0-a2m and even coefficients a1-a2m-1) and added (adders 35 and 36), the n-stage shift register being divided into a plurality of shift registers (even-order shift register of filter 51 and odd-order shift register of filter 52; col. 4, lines 35-41), and each divided shift register being time-divisionally driven (timing control circuit 54; col. 4, lines39-41) in synchronization with the input data (filter operation of the

even- and odd-order digital filters being synchronous with the shift operation of the shift register; col. 8, lines 63-66).

Claim Rejections – 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomimitsu (US 4777612) as applied to Claim 1 above, and further in view of Matsudera et al. (US 6198649 B1).

As to **Claim 2**, the claimed the claimed nonrecursive digital filter corresponds with subject matter mentioned in the rejection of Claim 1 above, similarly applicable hereto. Claim 2 further specifies the division of the shift register of the nonrecursive digital filter of Claim 1. However, Tomimitsu is silent on the division of the shift register into two shift registers each having n/2 stages (bits).

In disclosing a semiconductor device, however, Matsudera et al. shows an n-stage shift register being divided into first and second shift registers each having n/2 stages (a shift register section comprising a first shift register corresponding one for one even bits and a second shift register corresponding one for one with odd bits of the serial data, the first and second shift register being arranged independently: col. 6, lines

41-46), one of the first and second shift registers performing a shift operation at a rising edge of a shift clock, and the other of the first and second shift registers performing a shift operation at a falling edge of the shift clock (four-stage FF circuits (shift register) 9 for odd bits of the data and four-stage FF circuits (shift register) 10 for even bits of the data, triggering of the rising edges and falling edges of a clock signal, respectively; col. 13, lines 35-37 and 48-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Matsudera et al. into the method of Tomimitsu because this division of the shift register into two sections and using both rising and falling edges of the clock for triggering would provide for the operating speed to be increased, the power dissipation to be reduced, and the chip size to be reduce due to integrated circuit implementation (col. 7, lines 3-5).

6. Claims 3 - 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomimitsu (US 4777612) in view of Matsudera et al. (US 6198649 B1) as applied to claims 1 and 2 above, and further in view of Lomp et al. (US 6272168 B1).

As to **Claims 3** and **4**, the claimed nonrecursive digital filter corresponds with subject matter mentioned in the rejection of claims 1 and 2 above, similarly applicable hereto. Claim 3 extends the features of the nonrecursive filter to accommodate its application in a communication system. However, both Tomimitsu and Matsudera et al. are silent on these additional features.

However, Lomp et al. discloses, in an adaptive vector correlator (Fig. 8a) and

adaptive matched filter (figs. 8d and 16, col. 23, lines 44-48 and 56-58) for despreading, a shift registers to which a spreading-code sequence is input and a shift clock is inputted (register 872, Fig. 8d; register 1820, Fig. 16); a reference-code register that stores n reference codes (a memory providing a code sequence; col. 3, lines 53-56; code memory 222 storing a code sequence; col. 10; lines 18-22); multiplication device that multiplies (multipliers 1801-1811; col. 30, lines 59-61) an output of each stage of the shift register by the weighing factors (w1-wL, col. 23, lines 63-67; w1-w11, col. 30, lines 59-61); and a correlation-strength calculation device that adds multiplication results (adder 876; Fig. 8d; col. 24, lines 1-2; adder 1830, Fig. 16; col. 31, lines 1-5) to output a correlation strength. Further, the division of shift registers into stages and using both rising and falling edge of the shift clock for loading the shift registers is well known mechanism in the art for increasing the operation speed, and the same is true and implied for selections devices that are needed to select and out put the odd-numbered and the even-numbered stages of the reference-code register. Furthermore, using multiplexers to select from a number of input data as well as using exclusive-OR gates to implement multiplication operations is also well known in the art.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lomp et al. into the method of Tomimitsu and Matsudera et al. because it provides for a CDMA transceiver with an adaptive vector correlator and adaptive matched filter wherein the division of the reference code and the shift register into two (odd- and even-stages) and using both rising and falling edges of the clock for triggering would provide for the operating speed

to be increased, the power dissipation to be reduced, and the chip size to be reduced in an integrated circuit implementation as mentioned in the rejection of Claim 2 above (Matsudera et al.; col. 7, lines 3-5).

As to **Claim 5**, the claimed radio communication unit employing a CDMA method for performing operation corresponds with subject matter mentioned in the rejection of claims 1 - 4 above, similarly applicable hereto. Furthermore, Lomp et al. also teaches that the CDMA system comprising an RF receiving section (RF receiver 950; col. 29, lines 50-55), a demodulation section (the CDMA demodulator; col. 5, line 41-43), a correlation section that performs an inverse spectrum conversion (dispreading; col. 11, lines 1-3) and implies the need for a baseband demodulation of the received signal (col. 35, lines 21-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lomp et al. into the method of Tomimitsu and Matsudera et al. because it provides for a CDMA radio communication unit wherein the matched filter of its correlator would provide for increased operating speed and reduced power dissipation as mentioned in the rejection of Claim 2 above (Matsudera et al.; col. 7, lines 3-5).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomimitsu (US 4777612) in view of Matsudera et al. (US 6198649 B1) and Lomp et al. (US 6272168 B1) as applied to claims 1 - 5 above, and further in view of Tayebi et al. (US 6373827 B1).

As to **Claim 6,** the claimed radio communication unit corresponds with subject matter mentioned in the rejection of claims 1 - 5 above, similarly applicable hereto. However, Tomimitsu, Matsudera et al. and Lomp et al. are all silent on the system including a packet processing section.

However, Tayebi et al. further discloses a wireless radio communication system in a local area network (col. 4, lines 57-62) wherein a packet processing section that performs packet processing according to the received data (col. 17, lines 1-2; col. 17, lines 59-61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tayebi et al. into the method of Tomimitsu, in view of Matsudera et al. and Lomp et al., because it provides for a CDMA radio communication in a LAN wherein the matched filter of the correlator would provide for increased operating speed and reduced power dissipation as mentioned in the rejection of Claim 2 above (Matsudera et al.; col. 7, lines 3-5).

Other prior art cited

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Asai et al. (US 4817025) discloses a digital filter of non-cyclic type.

Northam (US 4369499) discloses a linear phase digital filter for filtering a data signal.

Ovens et al. (US 5381455) discloses an interleaved shift register.

Rosenberg (US 5493522) discloses a fast arithmetic modulo divider where both the rising edge and trailing edge of a clock pulse are used for triggering registers.

Fukasawa et al. (US 5533012) discloses a CDMA system with improved utilization of upstream and downstream channels.

Contact information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamshid Goshtasbi-G., whose telephone number is (571) 272-3012. The examiner can normally be reached on M-F 8:00/4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAYANTI PATEL
SUPERVISORY PATENT EXAMINER

Jamshid Goshtasbi-G.
Examiner
Art Unit 2637